## CLAIMS

What is Claimed is:

1. An ICE (in circuit emulation) system for debugging microcontroller code comprising:

a computer system for controlling a debugging process;

a microcontroller installed on a test circuit, the microcontroller configured to run microcontroller code;

an ICE coupled to the computer system, wherein the ICE emulates the microcontroller, and wherein the ICE is configured to run the microcontroller code cooperatively with the microcontroller to implement the debugging process; and

a debug interface included in the microcontroller for communicatively coupling the microcontroller and the ICE, the interface configured to enable data transmission when the microcontroller is operating at a reduced speed and to disable data transmission when the microcontroller is operating at a normal speed.

2. The system as recited in Claim 1 wherein the test circuit is a POD.

3. The system as recited in Claim 1 wherein the ICE includes a field programmable gate array (FPGA) where the microcontroller is emulated.

4. The system as recited in Claim 1 wherein the debug interface performs I/O operations with the ICE for the microcontroller.

5. The system as recited in Claim 1 wherein the low speed is 3 Mhz or lower.

6. The system as recited in Claim 1 wherein the normal speed is 24 Mhz or above.

7. The system as recited in Claim 1 further comprising:

a CAT 5 cable for communicatively coupling the ICE and the debug interface.

8. An ICE (in circuit emulation) method for debugging microcontroller code comprising:

a) initializing a first memory of an ICE and a second memory of a microcontroller with microcontroller test code;

b) executing the microcontroller test code on the microcontroller and on the ICE simultaneously;

c) decreasing an operating frequency of the microcontroller from a normal speed to a reduced speed, the decreasing commanded by the ICE during an execution halt;

d) while at the reduced speed, transmitting debugging commands between the ICE and the microcontroller via a debug interface of the microcontroller; and

e) increasing the operating frequency from reduced speed to normal speed after the debugging commands are transmitted.

9. The method of Claim 8 further comprising:

executing the microcontroller test code on the microcontroller and the ICE in lock step.

10. The method of Claim 8 further comprising:

increasing the operating frequency from reduced speed to normal speed after a debugging process implemented by the debugging commands is complete.

11. The method of Claim 8 wherein the increase in the operating frequency from reduced speed to normal speed is commanded by the ICE.

12. The method of Claim 8 further comprising:

initiating code execution on the microcontroller by transmitting a command from the ICE after increasing the operating frequency from reduced speed to normal speed.

13. The method of Claim 8 wherein the microcontroller is installed in a POD.

14. The method of Claim 8 wherein the ICE includes a field programmable gate array (FPGA) for emulating the microcontroller.

15. The method of Claim 8 wherein the debug interface performs I/O operations with the ICE for the microcontroller.

16. The method of Claim 8 wherein the reduced speed is 3 Mhz or lower.

17. The method of Claim 8 wherein the normal speed is 24 Mhz or above.

18. An ICE (in circuit emulation) system for debugging microcontroller code comprising:

a microcontroller installed on a test circuit, the microcontroller configured to run microcontroller code;

an ICE including a field programmable gate array (FPGA) for emulating the microcontroller, wherein the ICE is configured to run the microcontroller code in lock step with the microcontroller to implement a debugging process; and

a debug interface included in the microcontroller for communicatively coupling the microcontroller and the ICE, the interface configured to enable data

transmission when the microcontroller is operating at a reduced speed for transmitting debugging commands between the ICE and the microcontroller via the debug interface, and to disable data transmission when the microcontroller is operating at a normal speed after the debugging commands are transmitted.

19. The system as recited in Claim 18 wherein the debug interface performs I/O operations with the ICE for the microcontroller.

20. The system as recited in Claim 18 wherein the low speed is 3 Mhz or lower.

21. he system as recited in Claim 18 wherein the normal speed is 24 Mhz or above.